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Carbon Nano Tube Field Effect Transistor Based 4-Bit Full Adder Cell

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Authors' contributions

This work was carried out in collaboration between both authors. Author CJ designed the study, performed the statistical analysis and managed literature searches. Author SSG read and approved the final manuscript.

Original Research Article

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ABSTRACT

Addition is considered as the basic operation for every digital circuit or system, digital signal processing and control system. The fast and accurate operation of any digital system is mainly influenced by the performance of its resident adders. In this paper a 4-bit full adder is proposed using carbon nanotube field effect transistor which is energy efficient, operates at high speed and low voltage and consumes ultra low power. The full adder cell is designed using 48 transistors. The proposed technique has been examined at voltage 0.8V. The simulation results taken on HSPICE show that this module has given more than 42% in power savings over conventional Complementary Metal Oxide Semiconductor (CMOS) adder and 56% is faster.

Keywords: Basic gates; full adder; carbon nanotube field effect transistor; carbon nanotube.

1. INTRODUCTION

In the last few years, the technology based on silicon has been improved greatly by downscaling MOSFETs (Metal Oxide Semiconductor Field Effect Transistor), which has resulted in better device performance and density. But, still there are some problems to scaling, such as diffusion areas will no longer be separated by low doped channel region,

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the gate oxide thickness will fall below the tunneling limit, the short channel effects, very high leakage power consumption and the large parametric variations, physical limitations of miniaturization of silicon based circuits [1] So, it is necessary to extend or complement traditional silicon technology. Several materials have been explored as replacement of silicon channel and source/drain regions such as Ge, III-V compound semiconductors, nanowires, graphene nanoribbons and carbon nanotubes [2]. Out of all these, nanotechnology avoids most of the fundamental limitations or shortcomings for conventional silicon devices. Nanoelectronics i.e. branch of nanotechnology based on electronics is a field of nanotechnology that is producing nanoscale machines and systems efficiently, such as, nanoparticles etc. The most promising and feasible nano-technologies is CNT (Carbon Nanotube) based transistors called as Carbon nano tube field effect transistor (CNFET) [3,4,5]. As the adders are major parts of any computational circuit for implementing any arithmetic or mathematical operations such as subtraction, addition, multiplication or even logarithmic functions. Therefore, increasing the efficiency of an adder using CNFET will affect the performance of whole system [1].

2. CARBON NANOTUBE

Carbon Nano Tubes (CNT) are the sheets of graphene i.e. an isotope of carbon; rolled into tubes. Depending on the chirality (i.e., the direction in which the graphite sheet is to be rolled), the carbon nanotubes can either be single walled or double walled [1]. Further the single walled cabon nanotube can be classified as metallic or semiconducting. Since the discovery of CNT in 1991 by S. Iijima, significant applications of it have been observed in different fields because of its characteristics [6].

CNTs have special or extraordinary electronic, thermal and mechanical properties that can be implemented for the future integrated circuit applications [7]. The special characteristics of CNT such as high mobility of electrons, high I_{on}/I_{off} ratio and their unique one or single dimensional band structure which suppresses back scattering and near ballistic or ballistic operation has made it the most promising device for the creation of transistors on a scale smaller than that can be achieved with silicon [8].

3. CARBON NANO TUBE FIELD EFFECT TRANSISTOR

Transistors that are having carbon nanotubes as their channel are called CNFET (Carbon Nanotube Field Effect Transistor). A semiconductor or silicon based carbon nanotube (CNT) is good for using as channel of field effect transistors and it is the potential successor to silicon MOSFETs (Metal Oxide Semiconductor Field Effect Transistor). The voltage applied to gate can control or manage the electrical conductance of the CNT (Carbon Nano Tube) by making changes in electron density in the channel. By the use of appropriate value of diameter suitable threshold voltage for CNFET transistor can be achieved. The threshold voltage (V_{TH}) of the CNFET is directly proportional to the inverse of the diameter (d) of CNT and can be expressed as [1]:

$$V_{TH} = 0.42/ d\ (nm) \quad (1)$$

For the Carbon Nano Tube with chirality (n, m) and a as lattice the diameter (D_{CNT}) is [1]:

$$D_{CNT} = (a\ (n^2 + nm + m^2)^{1/2})/ \pi \quad (2)$$

Less power and high velocity of this nano tube based transistor has encouraged the digital circuit designers to use it for their designs. Since the I-V characteristics of CNFETs are quite similar to silicon MOSFET, most of MOS circuits can be transformed to a CNFET based design [4]. CNFETs in comparison with MOSFET transistors have less size and more scalability and this is the feature that makes it suitable for the displacement of technology. Recently, some circuit or design applications have been presented or reported based on CNFETs, i.e. ring oscillators, invertors, multiple valued reasonable circuits, accounted circuits, and logic gates [7].

4. PREVIOUS WORKS

As full adder is one of the major part of every processor in which the central part of digital computing lies and which take part in the arithmetical and logical unit(ALU), floating point unit(FPU) and address generation circuit as shown in Fig. 1.

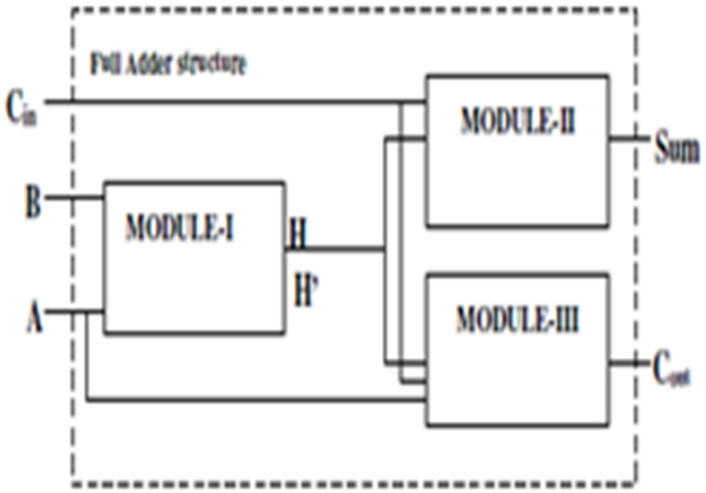

Fig. 1. Block diagram of full adder

Thus if the performance of this part is improved, it is to improve the total performance dramatically. Logic style diversity has motivated designers to implement full adders in different logic styles or sometimes in combined styles, called as the Hybrid logic style. Different logic styles have different properties. For example, they may be either full swing or non- full swing [9,10,11]. Amongst different designs, transistor count varies. There are also different types of adders available depending upon the method of carry generation, which are, Ripple carry adder(carry propagate adder); the adder used for the purposed 4-bit full adder, Carry skip adder, Multi-operand adder, Carry look-ahead adder, Manchester chain adder, Carry select adders, Pipelined parallel adder, Carry save Adder and Pre-Fix Adders[12].

Similarly, different designs of 1-bit full adders are available using carbon nano tube field effect transistor. An overview of previous networks is given here to provide enough background for the reader to follow the rest of the material. The first design as shown in Fig. 2; CNFET FA1 has 7 capacitors and 8 transistors. Next design which is shown in Fig. 3; CNFET FA2 has improved the circuit parameters by reducing the number of the capacitors

with 2 stages. The third design i.e. the design of Fig. 4; CNFET FA3 uses 8 capacitors and 10 transistors. This design was implemented by minority, NAND and NOR function. All these designs when cascaded to make a 4-bit adder results in the more consumption of power and larger delay compared to the one which has been chosen here to purpose a new 4-bit adder [1,4].

Ternary logic has inherently the potential of high computational speed in comparison with conventional binary logic. As shown in Fig. 5 a new low-transistor-count, high-speed ternary half adder in which Carbon nanotube field effect transistors are utilized is given. Unique characteristics of this technology provide multi-Vt circuitry with the flexibility which is highly essential for MVL designs. The given structure also benefits from high driving power and capability of operating in low voltages. It has only 26 transistors [13].

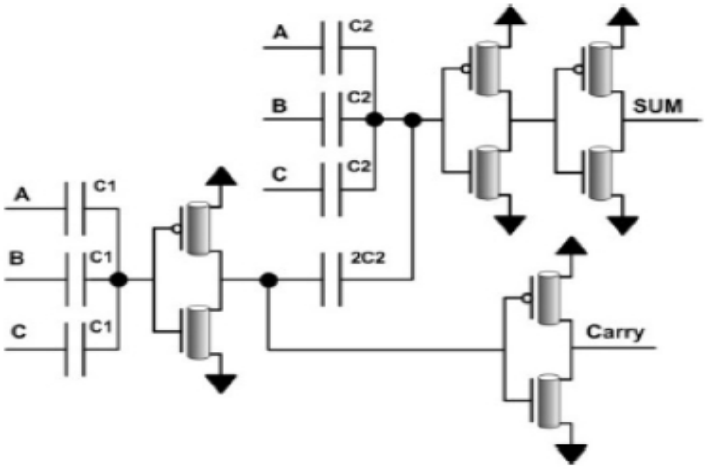

Fig. 2. CNFET FA1

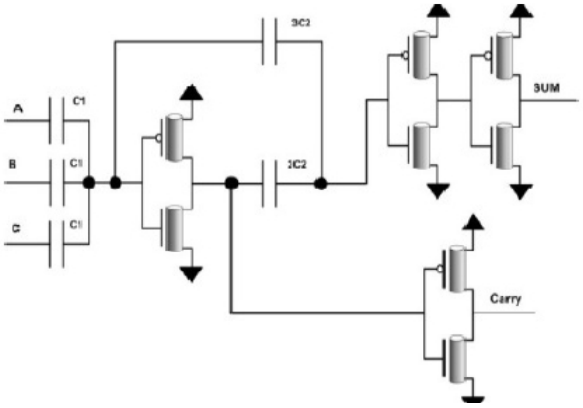

Fig. 3. CNFET FA2

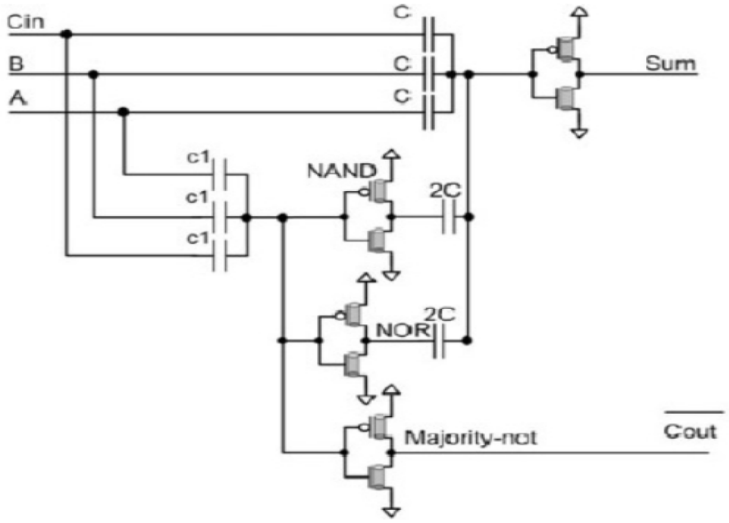

Fig. 4. CNFET FA3

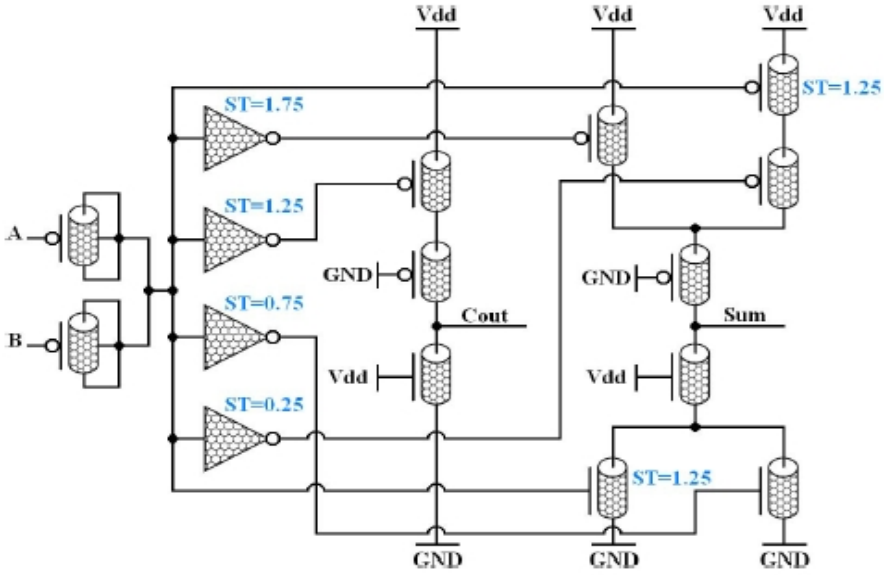

Fig. 5. Ternary adder

5. SOLUTION AND METHODOLOGY

After observing all the design the one which is presented here in Fig. 8 has been selected to design a 4- bit adder by following the Ripple carry ahead methodology as shown in Fig. 9. In this design a MOS-CNFET device is implemented in three levels. In first level (CNFET_L1) the intrinsic behavior of MOS-CNFET has been modeled. In level 2 (CNFET_L2) the device nonidealities have been included and in the top level of this hierarchical modeling (CNFET_L3), multiple CNTs for each MOS_CNFET device are allowable. This design does not contain any capacitor. The current sources and the trans-capacitance network are two

main parts of the CNFET_L1. Semiconducting sub-bands current, metallic sub-bands current and leakage current are three current sources considered for CNFET model.

The transistor count is very low i.e. 12. The low transistor count results in small size of the single module. Hence the overall area occupied by the 4-bit module will also be less.

This Transmission Gate Full Adder Cell is based on XOR/XNOR and transmission gates as shown in Fig. 6.

The following equations describe that how to carry (cout) and sum signals are generated in the single module [2].

$$Sum = (A \text{ XOR } B) \text{ CBAR} \Rightarrow (A \text{ XOR } B) C \quad (3)$$

$$Cout = (A \text{ XOR } B) C \Rightarrow (A \text{ XOR } B) A \quad (4)$$

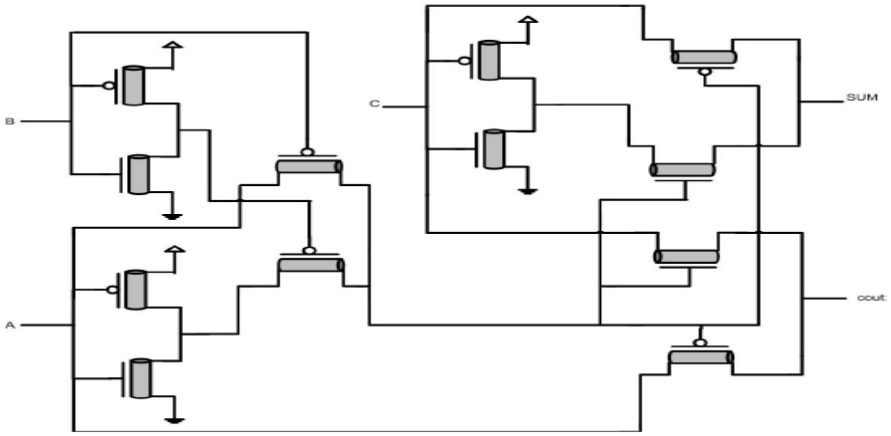

Fig. 6. Transmission gate adder

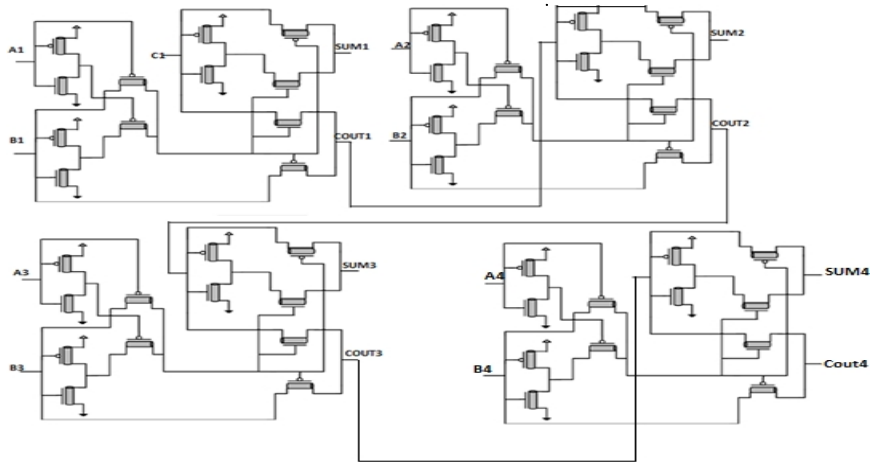

Fig. 7. Proposed 4-bit adder

Transmission gates are used in this design to avoid the threshold voltage loss in output at the cost of using more transistors (i.e., six transistors). As mentioned above, CNFETs adjust voltage threshold toward zero by increasing the diagonal of CNT. Therefore, the transmission gates can be replaced by pass transistors as shown in Fig. 7. After that by substituting two pCNFETs by two nCNFETs obviates required inverter from the circuit for transforming XOR to XNOR . this design gives the final 1-bit adder as shown in Fig. 8.

The design is then cascaded to design the 4-bit adder using ripple carry ahead technique. Thus by selecting the parameters of the nanotubes used in the transistors and operating voltage, the following results have been obtained.

6. RESULTS AND DISCUSSION

The circuits are compared by power consumption, propagation delay and then power delay product (PDP). First the result of 1-bit adders is compared. And then the 4-bit adder designed using the CNFET FA4 has been compared with the other previously designed 4-bit adders using MOSFETs and Different Carry configuration. The simulation is done at 0.8V. The HSPICE simulator has been used for simulating various circuits. The compact model of CNFET has been used. Table 1 shows the value of power, delay and PDP (Power Delay Product). Delay is measured from middle of the input voltage swing to the middle of the output voltage swing. In Figs. 10,11,12,13 the output is shown in the form of waveform, for which the voltage is measured at various nodes.

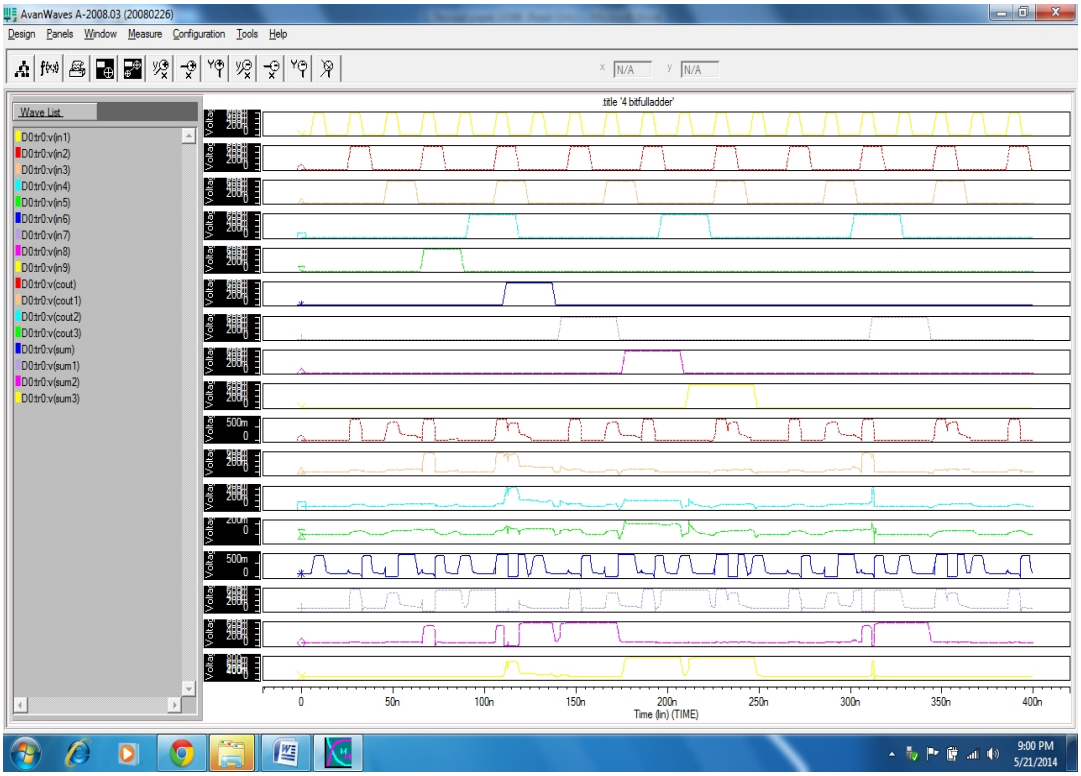

Fig. 8. Output waveforms of CNFET FA-4

Simulation results in Table 1 and Table 2, indicate that the delay belonging to the proposed 4-bit Full Adder cell is very small. PDP is calculated as a trade-off between power consumption and delay. It is a measure of total performance of a circuit.

Table 1. Simulation results for 1-bit adder

Design	Power	Delay
CNT-FA1[1]	4.71E-07	8.82E-11
CNT-FA2[1]	7.12E-07	7.51E-11
CNT-FA3 [4]	7.12E-07	7.51E-11
Ternary Adder[13] at 0.75v	306.9E-07	27.29E-11
Proposed Adder	4.80E-07	1.29E-10

Table 2. Simulation results for 4-bit adder

Design	Power (Watt)	Delay (Sec)	Power Delay Product
4-bit carry ripple adder using MOSFET [12]	87.5E-02	72.1E-09	63.1
4-bit carry look-ahead adder using MOSFET	1.5	93.54E-09	98.2
4-bit carry select adder using MOSFET [12]	1.7	24.72E-09	40.5
4-bit Manchester adder using MOSFET [12]	1.9	27.58E-09	29.9
4-bit CNFET FA4 [12]	17.2E-07	6.5490E-08	1.9E-13

7. CONCLUSION AND FUTURE SCOPE

In this paper an improved 4-bit full adder cell has been purposed using Carbon Nano Tube Field Effect Transistor. Use of CNFETs as a novel architecture improves the efficiency. This design has been implemented using majority-not function and using majority-not circuit design as AND and OR functions by changing threshold voltage of CNFETs to produce intermediate signals. It controls all the three stable output voltage values by controlling the appropriate Carbon Nano Tube Field Effect Transistors. To achieve an improved Full Adder circuit design, all the CNFETs have been used to activate the adequate guidance path and to disable all the other paths to the output. To evaluate the performance of the design delay, power and PDP factors are compared with some of the state-of-the-art MOS and CNFET-based designs. Simulations have been performed on HSPICE by using CNFET technology in practical voltage at 0.8v. Simulation results illustrate improvements in terms of delay and PDP in comparison to previous MOSFET and CNFET designs.

COMPETING INTERESTS

After this I would like to design an 8-bit full adder using Carbon Nano Tube Field Effect Transistors which would be far efficient than the existing MOSFET based 8-bit adders.

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